REMARKS

Claims 1, 2, 4-5, and 7-14 remain in the application for consideration of the Examiner with Claims 3, 6, 15-21 standing canceled and with Claims 22-26 standing withdrawn.

Reconsideration and withdrawal of the outstanding rejections and objections are respectfully requested in light of the above amendments and following remarks.

The drawings were objected to under 37 CFR 1.84.

The specification has been amended to eliminate the reference numbers.

The drawings are in full compliance with 37 CFR 1.84.

The drawings are objected to under 37 CFR 1.83.

The Examiner's attention is directed to column 32 et seq.

Here the specification describes how the feedback loop is shown in the drawings.

The drawings are in full compliance with 37 CFR 1.83.

Claims 1-21 were rejected under 35 U.S.C. §112, second paragraph, as being indefinite.

By the instant amendment, some of the Examiner's comments have been incorporated into the amended claims.

However this rejection is traversed in part.

The Examiner alleges that the second switch providing a feedback path from the second circuit to an input of the second circuit is indefinite. Specifically the Examiner requests were the feedback starts and ends.

Applicants respectfully submit that this is indicated by the to and from language of the claim.

Next, the Examiner questions if the integrated circuit operates in the voltage mode only.

Applicants respectfully submit that only is not part of the claim language.

The Examiner questioned what determines the integrated circuit to operate in a voltage mode.

Applicants respectfully submit that the claim clearly set forth at the first and second switches performs these tasks.

With respect to Claim 15 and Claim 20, the cancellation of Claims 15-21 obviates the rejections of these claims.

Turning now to the art rejections, Claims 1-4, 7-10, 13-17, 20, and 21 were rejected under 35 U.S.C. §103 as being unpatentable over Kondou in view of Stuebing, and Claims 5, 6, 11, 12, 18, and 19 were rejected under 35 U.S.C. §103 as being unpatentable over Kondou in view of Stuebing and in view of the ordinary skill in the art.

These rejections are respectively traversed.

It is respectfully submitted that Kondou does not disclose or suggest the presently claimed invention including the second circuit for mirroring a current in the first circuit at a predetermined mirroring ratio to provide drive currents to the piezo element in independent Claim 1. Albeit, defined as the second integrated circuit means for mirroring

a circuit in the integrated circuit means at a predetermined mirror ratio to provide drive currents to the piezo element in independent Claim 8.

The Examiner alleges that Kondou discloses a first current source 106 and a second current source 107.

However, these circuits are not mirrored together.

It is respectfully submitted that Stuebings does not disclose or suggest the presently claimed invention including the second circuit for mirroring a current in the first circuit at a predetermined mirror ratio to provide drive currents to the piezo electric element in the varies forms in independent Claims 1 and 8.

Stuebing does not disclose a piezo electric element.

Applicants agree with the Examiner that Stuebings and Konduo do not disclose the mirror ratios of 10 to 1 and 6.125 to 1.

Applicants respectfully traverse the allegation that it is within the skill of ordinary skill in the art to determine these ratios.

In this light, a teaching from the prior art is respectfully requested.

It is respectfully submitted that Claims 1, 2, 4-5, and 7-14 patentably define over the applied references.

In light of the above, it is respectfully submitted that the present application is in condition for allowance, and notice to that effect is respectfully requested.

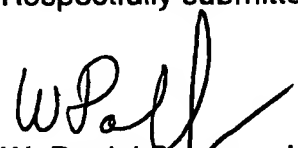
While it is believed that the instant response places the application in condition for allowance, should the Examiner have any further comments or suggestions, it is

respectfully requested that the Examiner contact the undersigned in order to expeditiously resolve any outstanding issues.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE."

To the extent necessary, Applicant petitions for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668.

Respectfully submitted,



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the specification:

Paragraph 0028 has been amended as follows:

[0028] A microcontroller 34 is typically provided to control the DSP 30 as well as the interface controller 36 to enable data to be passed to and from the host interface (not shown) in known manner. A data memory 38 may be provided, if desired, to buffer data being written to and read from the disk 12 ~~18~~.

Paragraph 0032 has been amended as follows:

[0032] The mode of the circuit is controlled by two MOS transistors 60 and 62, which have a selection signal applied to their respective gates on lines 64 and 66. When driving the piezo motor in voltage mode, the 1X output 52 of the OTA 46 is disabled and the nX output 54 is used to create a voltage feedback loop through MOS transistor 62. In charge mode, MOS transistor 60 conducts, coupling the nX output 54 to analog ground, AGND 74 ~~72~~.

In the claims:

Claims 15-21 have been canceled.

Claims 1, 10, 13, 15, 17, and 20 have been amended as follows:

1. An integrated circuit for providing drive signals to a piezo element of a milli-actuator device in a mass data storage device, comprising:

a first circuit for receiving head position control signals and for providing a charging current to a sense capacitor in response thereto;

wherein said first circuit is powered by a voltage supply that is measured with respect ~~referenced~~ to a substrate potential; and

a second circuit for mirroring a current in said first circuit at a predetermined mirror ratio to provide drive currents to said piezo element.

10. The milli-actuator driver of claim 8 wherein said voltage supply is not ~~a voltage supply other than~~ a voltage supply for said piezo element.

13. The milli-actuator driver of claim 8 further comprising:

a first switch connected to ~~selectively~~ disable said first integrated circuit; means

a second switch connected to form ~~selectively provide~~ a feedback path from said second integrated circuit means to an input of said second integrated circuit; means

wherein when said first and second switches are ~~selectively~~ operated, said integrated circuit operates in a voltage mode.

15. An integrated circuit for providing drive signals to a piezo element of a milli-actuator device in a mass data storage device to position a data head thereof, said integrated circuit comprising:

a current mirror;

said current mirror comprising:

a first current mirror portion;

said first current mirror portion being configured to receive head position control signals from a head position sensing circuit;

said first current mirror portion being configured to provide a first current in response to said head position control signals for connection to a capacitor;

said first current mirror portion being powered by a voltage supply that is referenced to a substrate potential;

a second current mirror portion;

said second current mirror portion being configured to mirror said first current at a predetermined mirror ratio; and

said second current mirror being configured to provide drive currents for connection to said piezo element.

17. The integrated circuit of claim 15 wherein said voltage supply is not ~~a voltage supply other than~~ a voltage supply for said piezo element.

20. The integrated circuit of claim 15 further comprising:

a first switch connected to ~~selectively~~ disable said first current mirror portion

a second switch connected to provide ~~selectively provide~~ a feedback path from said second current mirror portion o an input of said second current mirror portion

wherein when said first and second switches are ~~selectively~~ operated, said integrated circuit operate in ~~sin~~ a voltage mode.